WHAT IS CLAIMED IS:

1. A method for manufacturing composite substrates for semiconductor devices, the method comprising:

providing a metal substrate, the metal substrate having a first diameter and having a bonding surface;

bonding a plurality of tiles overlying the bonding surface, each of the tiles being coupled to a portion of the bonding surface, each of the tiles having a shape and size to be able to form an array configuration;

elevating a temperature of the plurality of tiles and metal substrate;

forming a eutectic bond between each of plurality of tiles and portion of the bonding surface, whereupon the elevating of the temperature is provided while each of the tiles is substantially stationary relative to the metal substrate;

forming a plurality of active devices on each of the plurality of tiles;

forming a plurality of openings through each of tiles, each of the openings traversing through a portion of one of the tiles through a portion of the eutectic bond to a portion of the metal substrate to form a via structure;

forming an interconnect layer to connect the portion of the one of the active devices through the portion of the tile through the eutectic bond to the portion of the metal substrate;

whereupon the interconnect layer that connects the portion of one of the active devices through the portion of one of the tiles through the portion of the eutectic bond to the portion of the metal substrate.

2. The method of claim 1 wherein the forming of the plurality of openings in each of the tiles further comprises coating the plurality of active devices using a photolithographic material and patterning the coating to form regions corresponding to the openings.

3. The method of claim 2 wherein the patterning comprises an etching process.

4. The method of claim 1 wherein each of the tiles comprises an entity selected from gallium arsenide, indium phosphide, gallium nitride, and silicon carbide.

5. The method of claim 1 wherein each of the openings is a via structure.

6. The method of claim 1 wherein the eutectic bond is provided using an alloy selected from a low melting temperature metal including indium, tin and an oxidation-resistant metal.

7. The method of claim 1 wherein the array configuration is an N by M array of the tiles, each of the tiles being coupled to another tile.

8. The method of claim 1 wherein each of the openings is characterized by an aspect ratio of greater than 2 to 1.

9. The method of claim 1 wherein the interconnect layer comprises gold over platinum over titanium.

10. The method of claim 1 wherein the interconnect layer comprises a barrier metal layer underlying a conductive layer.

11. The method of claim 1 wherein the metal substrate provides a ground plane.

12. A method of manufacturing bonded substrates, the method comprising:

providing a metallic substrate, the metal substrate having a predetermined thickness;

bonding a first thickness of compound semiconductor material overlying the metallic substrate;

reducing a thickness of the first thickness of compound semiconductor material to a second thickness; and

forming one or more via structures through a portion of the second thickness of compound semiconductor material to a portion of the underlying metal substrate, whereupon the via structure electrically connects to the metal substrate.

13. The method of claim 12 wherein the second thickness of compound semiconductor substrate is less than 100 microns.

14. The method of claim 13 wherein the second thickness of compound semiconductor material is unstable without the metal substrate.

15. The method of claim 13 wherein the via structure has an aspect ratio is greater than 2 to 1.

16. The method of claim 12 wherein the metal substrate is characterized by a first thermal expansion coefficient and the compound semiconductor is characterized by a second thermal expansion coefficient, whereupon the first thermal expansion coefficient is within a predetermined amount of the second thermal expansion coefficient.

17. The method of claim 12 wherein the predetermined amount is characterized to prevent any damage to the compound semiconductor through a temperature range from about room temperature to 550 Degrees Celsius.

18. The method of claim 12 further comprising processing the second thickness of compound semiconductor through one or more manufacturing processes for integrated circuits.

19. The method of claim 18 wherein the one or more manufacturing processes includes at least an alloying process to form a contact between the compound semiconductor and a metal layer.

20. The method of claim 19 wherein alloying process is an annealing process.

21. A method of manufacturing bonded substrates, the method comprising:

providing a metallic substrate, the metallic substrate having a predetermined thickness;

bonding a first thickness of compound semiconductor material overlying the metallic substrate;

reducing a thickness of the first thickness of compound semiconductor material to a second thickness; and

forming one or more trench structures through a portion of the second thickness of the compound semiconductor through a side opposite of a backside of the metallic substrate;

forming one or more metal structures within the one or more trench structures to form one or more respective via structures within the portion of the second thickness of

compound semiconductor material to a portion of the underlying metal substrate, whereupon the via structure electrically connects to the metal substrate.

22. A method of manufacturing bonded substrates, the method comprising:

providing a metallic substrate, the metal substrate having a predetermined thickness;

bonding a first thickness of compound semiconductor material overlying the metallic substrate;

reducing a thickness of the first thickness of compound semiconductor material to a second thickness; and

forming a trench region surrounding a portion of the second thickness of the compound semiconductor material; and

forming a conductive material within the trench region to isolate the portion of the second thickness of the compound semiconductor using the conductive material in the trench region and a portion of the underlying metallic substrate.

23. The method of claim 22 exposing an upper portion of the portion of the second thickness of the compound semiconductor.

24. The method of claim 22 further comprising forming an insulating layer overlying the exposed upper portion.

25. The method of claim 24 further comprising forming a metal layer overlying the insulating layer and connecting to the conductive material in the trench region to enclose the portion of the second thickness of the compound semiconductor.

26. A substrate structure for high frequency devices, the structure comprising:

a metallic substrate, the metallic substrate being a ground plane for a high frequency amplifying device operable at a frequency greater than 10 G Hz;

a compound semiconductor material bonded to the metallic substrate;

one or more via structures for ground connections formed within portions of the compound semiconductor material, the one or more via structures being electrically connected to the metallic substrate;

whereupon the one or more via structures are configured to provide a desired reactance to provide a universal ground reference, the universal ground reference is within a predetermined amount.

27. The structure of claim 26 wherein predetermined amount is less than one quarter of the wavelength of the operating frequency of the circuit.

28. The structure of claim 26 wherein the desired reactance ranges from about 0.01 ohm to about 1 ohm.

29. An integrated circuit device structure, the integrated circuit device structure comprising:

a metallic substrate, the metal substrate having a predetermined thickness and a predetermined thermal conductivity;

a thickness of compound semiconductor material bonded to a surface overlying the metallic substrate; and

a trench region disposed within a portion of the thickness of the compound semiconductor material and extending to a portion of the metallic substrate; and

a thermal conductive material formed within the trench region and thermally coupled to the portion of the metallic substrate, the thermal conductive material being coupled to the portion of the thickness of the compound semiconductor to redistribute thermal energy among the portion of the compound semiconductor, the thermal conductive material, and the metallic substrate.

30. The structure of claim 29 wherein the trench region surrounds the portion of the thickness of the compound semiconductor material.

31. The structure of claim 29 wherein the substrate is a heat sink.

32. The structure of claim 29 wherein the redistributed thermal energy provides the portion of the compound semiconductor free from one or more hot spots.